PERFORMANCE OF A 6 TO 18 GHz FREQUENCY TRANSLATOR UTILIZING GaAs MMIC 5-BIT DIGITAL PHASE SHIFTER

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ABSTRACT

More than 22 dB of carrier and spurious suppression over 6 to 18 GHz has been achieved for a translator employing MMIC phase shifter. Trade-off of maximum allowed amplitude and phase errors versus number of bits are analyzed. For spurious levels <-29.8 dBc, the amplitude and phase errors must be $\leq \pm 0.83$ dB and $\leq \pm 5.65$ degrees respectively.

INTRODUCTION

Frequency translation is utilized in ECM applications to generate a false target signal (Doppler shifted) in order to deceive a hostile radar system.

A frequency translator device shifts up or down the frequency of an input signal by some desired amount (usually less than a few hundred kilohertz). It provides output only at the shifted (translated) carrier frequency with minimum loss and ideally without generating any unwanted spurious frequencies.

Translators using phase shifters are based on the principle of phase modulation. When the phase angle of an input RF signal of frequency f_0 is varied linearly with time (having phase vs time slope corresponding to a frequency of f_m) then the frequency of the resultant output signal is "translated up" to (f_0+f_m) as depicted in Figure 1(a). It may be noted that for a negative slope of the phase function, the output frequency will be "translated down" to (f_0-f_m).

Ideal frequency translation can also be performed by using periodic "sawtooth" phase function, which repeats after a phase change of 360 degrees as shown in Figure 1(b). This technique is also known as Serrodyne frequency translation.

Practical translators are realized using a chain of digital phase shifters to approximate the continuous 0 to 360 degree sawtooth phase function by a stepped-phase shift or "staircase" as shown in Figure 1(c).

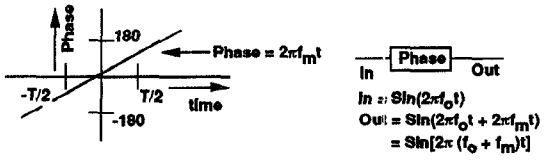

Figure 1(a). Linear Phase Function

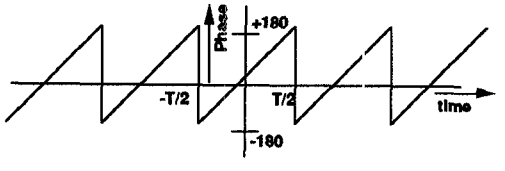

Figure 1(b). Serrodyne Phase Function

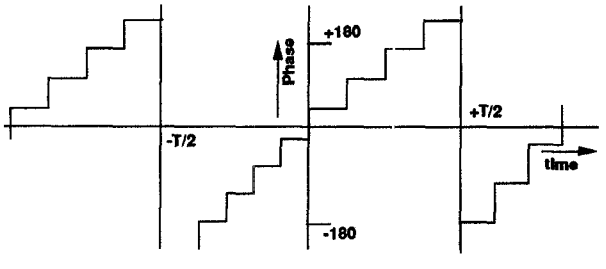

Figure 1(c). Staircase Approximation of the Serrodyne Phase Function

Characteristics of a frequency translator using phase shifters have been discussed [1-5] and performances reported over narrow bands. For example, over 7 to 11 GHz, spurious sideband suppression of 22 dB was reported in [3].

Frequency translators operating over the full 6 to 18 GHz are not currently available. Furthermore, although effects of amplitude and phase errors on various spurious sideband levels have been discussed [1-4], a

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quantitative trade-off of the two errors as function of number of bits is not available.

In the following, trade-off of maximum amplitude and phase errors that can be tolerated, as a function of number of bits, without exceeding the spurious levels (corresponding to ideal staircase) is provided. Performances over 6 to 18 GHz of the Raytheon's 5-bit MMIC phase shifter as frequency translator are presented.

Advantages of using the proposed MMIC based approach are for example: (i) single module wideband 6 to 18 GHz performance can potentially replace existing multiple-module, narrowband MIC designs and (ii) inherent lower cost of MMIC based design by eliminating significant touch labor in "tuning costs" that are currently incurred in the MIC PIN diode based narrowband designs.

CHARACTERISTICS OF A FREQUENCY TRANSLATOR BASED ON DIGITAL PHASE SHIFTERS

The staircase approximation of the ideal linear phase function results in unwanted spurious signals whose levels are determined by the following factors: (1) number of phase steps or number of phase bits, (2) insertion loss errors in the bits, (3) phase errors in the bits and, (4) switching time of the phase bits.

The following summarizes the characteristics of a frequency translator on the basis of Fourier analysis of the staircase approximation of the phase function of an RF signal [1-4]:

(i) When there are no amplitude and phase errors, it is found that the input frequency (f_0) and all undesired harmonics of f_m (translation frequency) are completely suppressed except those frequencies given by:

$$f_{out} = f_0 + C(1 \pm k.N)f_m = f_0 + C(n.f_m) \quad (1)$$

where, C = +1 or -1 for translation "up" or "down" respectively, N = number of phase steps, k = 0,1,2..., n = (1±k.N) = spectrum number and + or - corresponds to upper or lower sidebands. It may be noted that for binary 5-bit case, $N = 2^5 = 32$ and spectral components present are at n = -1 for downward translated carrier and spurious signals are at n = +31,+63, +35....and -33, -65, -97...etc.

The amplitudes of the spectral components given by equation (1) are expressed as:

$$C_n = [\mathrm{Sin}(\Pi/N)] / [(kN \pm 1)(\Pi / N)] \quad (2)$$

and are shown in Figure 2(a) for 5-bit approximations.

Figure 2(b) shows the worst spurious sideband level (corresponding to k = 1 in equation (2)) as function of number of ideal phase bits. For example, for a 5-bit or 32-step case, the spurious sideband levels cannot be less than -29.8 dBc with respect to the translated carrier. In general the worst spurious levels relative to the translated carrier are given by -20*Log(N-1) dBc, where N = number of phase steps.

(ii) Errors in the 180° phase bit degrades only the carrier and the even sidebands.

(iii) Errors in the 90° phase bit degrades only the odd sidebands spaced by $4f_m$.

(iv) Errors in the 45° phase bit degrades only the odd sidebands spaced by $8f_m$.

(v) Errors in the 22.5° phase bit degrades only odd sidebands spaced by $16f_m$ and so on.

By extending the Fourier analyses to the general case of including the amplitude and phase errors of the phase bits, effects of these errors on the spurious levels have been studied. A trade-off of the maximum amplitude and phase errors that can be tolerated (versus number of phase bits) without exceeding the spurious levels (corresponding to ideal staircase) is shown in Figure 2(c), where contours for each number of bits are plotted using amplitude errors as the x-axis and the phase errors as the y-axis. It is observed that for the 5 bit case (least significant bit = 11.25 degrees and ideal worst spurious = -29.8 dBc), the amplitude errors must be within ±0.83 dB and the phase errors must be within ±5.65 degrees (less than half the phase shift of the least significant bit).

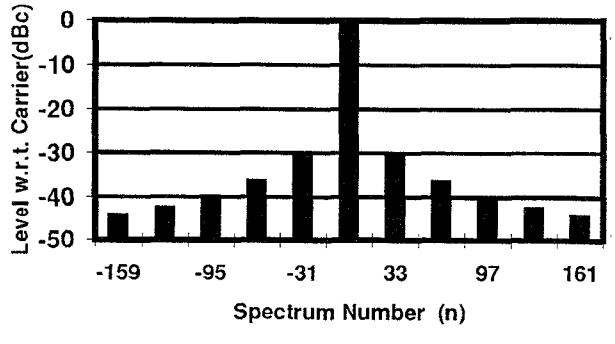

Figure 2(a). Ideal Spectrum of Translator Based on 5-Bit Phase Shifter

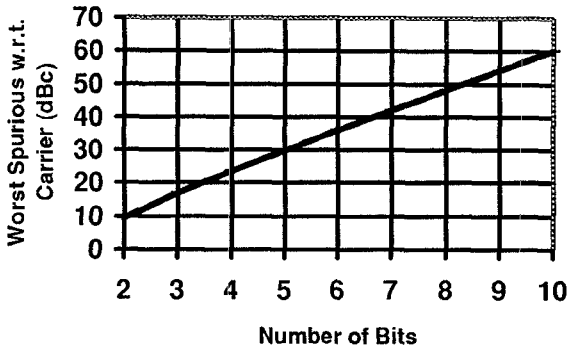

Figure 2(b). Ideal Spurious Suppression versus Number of Bits

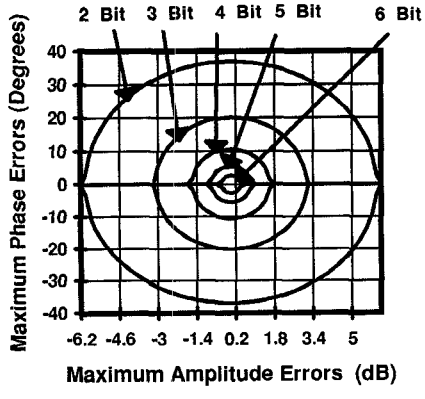

Figure 2(c). Trade-off of Maximum Amplitude and Phase Errors versus Number of Bits

PERFORMANCE OF MMIC 5-BIT PHASE SHIFTER AS A FREQUENCY TRANSLATOR

Figure 3(a) shows the layout of the Raytheon's 5-bit phase shifter. The design of this chip is based on high/low-pass filter circuit concept [6,7] and utilizes switching FETs to switch between phase states. At a particular phase state of each bit, a group of FETs are turned "ON" and another group of FETs are turned "OFF." In the second phase state of the bit, the first group of FETs are now turned off and the second group of FETs being simultaneously turned on. Thus, every phase bit requires two complementary control signals, i.e., when one is at 0 volts, the other is at pinch-off (typically less than -5V) and vice versa.

Figure 3(b) shows the block diagram of the frequency translator utilizing the MMIC 5-bit phase shifter chip shown in Figure 3(a).

The control signals for sequentially stepping through the 32 steps of the 5-bit phase shifter are generated using a 5-bit counting circuit followed by drivers using TTL HEX inverter gates of the advanced CMOS type. This approach allowed operation of the interface circuitry at high clock frequency close to 15 MHz, thus extending translation frequency limits to about 500 KHz.

Figure 3(c) shows a photograph of the translator circuit where the control and interface driver circuitry are realized on thick-film alumina substrate.

Performance of the 5-bit phase shifter was first evaluated by statically setting the control signals corresponding to each of the 32 steps of the phase shifter. Figures 3(d) and 3(e) show the insertion loss and differential phase shifts respectively of all the 32 steps of the phase shifter over 6 to 18 GHz.

The insertion loss of the phase shifter varies from a nominal 6 dB at 6 GHz to about 14 dB at 18 GHz with loss variation among the 32 states less than ±1.5 dB at a particular frequency. The errors in the differential phase shifts are quite large and measured to be less than ±10 degrees over the band of 6 to 18 GHz.

Performance of the phase shifter as frequency translator was then evaluated by dynamically changing the control signals and observing the output spectrum corresponding to a particular carrier frequency. Figure 3(f) shows a typical spectrum observed for input frequency of 6.5 GHz. The output signal is translated downward by about 300 KHz (the control circuit was driven at clock frequency of about 10 MHz). It is observed that the carrier and other unwanted sidebands are suppressed by more than 22 dB. Figure 3(g) shows similar performance for input frequency of 18 GHz.

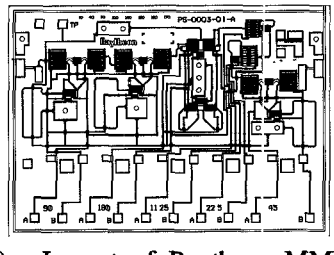

Figure 3(a). Layout of Raytheon MMIC 5-Bit Phase Shifter

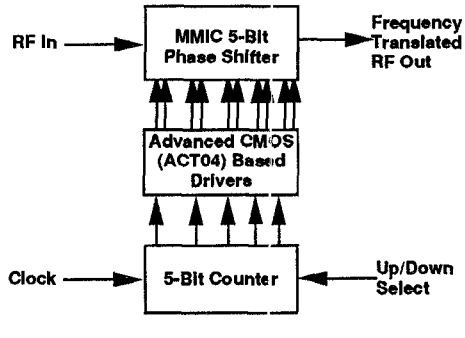

Figure 3(b). Block Diagram of the Frequency Translator

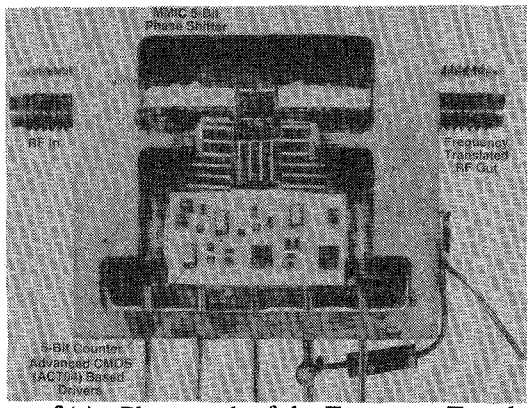

Figure 3(c). Photograph of the Frequency Translator

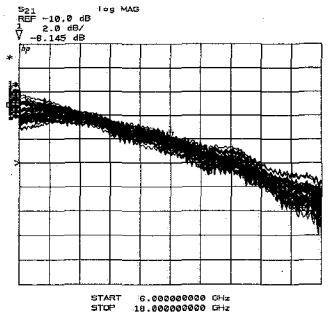

Figure 3(d). Insertion Losses of 32 States of the 5-Bit Phase Shifter

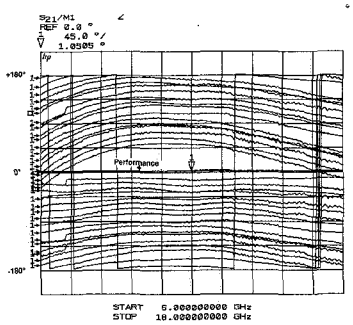

Figure 3(e). Differential Phase Shifts of 32 States of the 5-Bit Phase Shifter

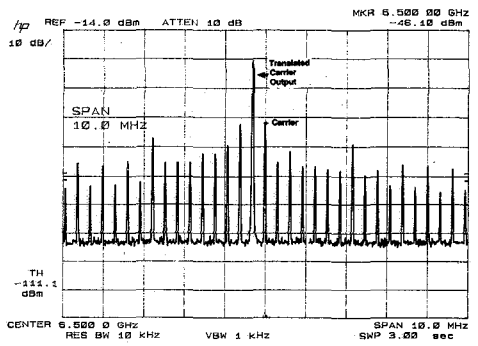

Figure 3(f). Measured Output Spectrum of the Frequency Translator at 6.5 GHz

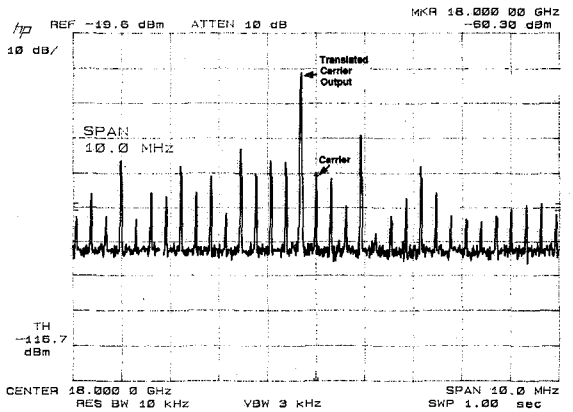

Figure 3(g) Measured Output Spectrum of the Frequency Translator at 18 GHz

CONCLUSIONS

A 5-bit GaAs MMIC phase shifter has been utilized to realize a frequency translator device which provided more than 22 dB of carrier and spurious suppression over 6 to 18 GHz. The counting and the driver circuits were realized using Advanced CMOS TTL devices allowing high speed operation with resulting translation frequency capability of 500 KHz.

A trade-off of the maximum amplitude and phase errors that can be tolerated (versus number of phase bits) without exceeding the spurious levels (corresponding to ideal staircase) is presented.

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